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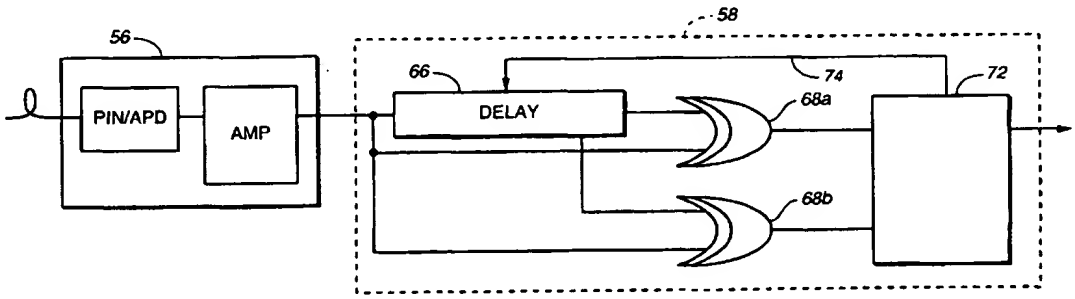
(54) Title: SIMPLE, HIGH-SPEED OPTICAL SIGNAL PATTERN AND PROTOCOL DETECTION



(57) Abstract: A pattern and protocol detector (50) includes an optical-to-electrical ("OE") converter (56) that receives a modulated beam of light. The modulation imposed upon the beam of light includes repetitive patterns. The detector (50) also includes a delay means (66) that receives the electrical-signal produced by the OE converter (56), and produces a temporally delayed replica of the received electrical-signal. The temporal delay in the electrical-signal introduced by the delay means (66) is selected to effect a matching of a repetitive pattern present in the modulated beam of light. The detector (50) also includes a combining circuit (68), preferably an Exclusive-OR gate, that receives both the undelayed and delayed signals and combines them to produce a low-frequency signal. The low-frequency signal, representing matching and mismatching between individual bits in the two signals, permits a digital-logic circuit (72) to produces a signal that indicates occurrence of the repetitive patterns.

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SIMPLE, HIGH-SPEED OPTICAL SIGNAL PATTERN AND PROTOCOL DETECTION

Technical Field

The present invention relates generally to optical telecommunication systems, and more particularly to detecting patterns and protocols in digital signals transmitted thereover.

Background Art

An optical, or photonic, crossconnect is a switching device used in optical telecommunication systems which permits coupling an incoming optical signal, received via any one of a number of input optical fibers, into any selected one of a number of output optical fibers. Furthermore, the coupling of the optical signal between any one of a number of input optical fibers and any selected one of a number of output optical fibers by the optical crossconnect occurs without the optical signal being converted into an electrical signal.

Optical telecommunication signals, such as those received by an optical crossconnect, are generally modulated in accordance with a protocol called Synchronous Optical Network ("SONET"). The SONET protocol is a standard for optical telecommunications transport formulated by the Exchange Carriers Standards Association ("ECSA") for the American National Standards Institute ("ANSI"), which sets industry standards in the U.S. for telecommunications and other industries. In brief, SONET defines optical carrier ("OC") levels and electrically equivalent synchronous transport signals ("STSs") for the fiber-optic-based transmission hierarchy. SONET defines a technology for carrying many signals of different capacities through a synchronous, flexible, optical hierarchy.

Any type of service, ranging from voice to high speed data and video, can be accepted by various types of SONET service adapters. In accordance with the SONET protocol, all such inputs are eventually converted to a base format of a synchronous STS-1 signal (51.48 Mbps or higher). Several synchronous STS-1s are then multiplexed together to form an electrical STS-n signal. After the "n" STS-1 signals have been multiplexed together, no

additional signal processing occurs except a direct conversion from electrical to optical to produce an OC-n signal.

The STS-1 signal employs a frame format. In general the STS-1 frame format can be divided into two main areas, transport overhead and the synchronous payload envelope ("SPE"). After, the payload has been multiplexed into the SPE, it can be transported and switched through the SONET without having to be examined and possibly demultiplexed at intermediate nodes. Thus, SONET is said to be service-independent or transparent. An entire STS-1 frame is transmitted every 125 microseconds, i.e. at an 8 KHz frame rate.

The SONET protocol provides a framing signal which occurs between each successive frames at the 8 KHz STS-1 frame rate. This framing signal consists of a number of successive bytes which repeat over and over the value $F6_h$ (hexadecimal). This first set of framing bytes is then followed by an equal number of successive bytes which repeat over and over the value 28_h. For example, the framing signal for an OC-48 SONET signal consists of forty-eight (48) bytes that repeat the $F6_h$ value, followed by forty-eight (48) bytes that repeat the 28_h value.

To prevent long sequences of a constant value from occurring in SONET frames, the data in each SONET frame is combined in an Exclusive-OR gate with a scrambling pattern that is 127 bits long for SONET, SDH, and IP over optical signal protocols. The combining of the scrambling pattern with the data in each SONET frame repeats over and over throughout all the data of the frame.

Thus, modulation imposed upon an optical telecommunication signal as described above for the SONET protocol includes first the repetitive pattern of the framing signal, and also the repetitive pattern of the scrambling pattern.

After an OC-n signal has been created by multiplexing together n STS-1 signals in the manner described above and the STS-n electrical signal converted to an optical signal, in traversing the fiber optic network the OC-n signal may pass through several regenerators before reaching its ultimate destination. If a failure occurs in the network, a device which detects the network failure continues transmitting data in accordance with the SONET protocol. However, th device

detecting the failure, e.g. a regenerator, transmits an Alarm Indicator Signal ("AIS"), i.e. a constant data value, all logical ones (1's), throughout the interval between the $F6_h$-28_h framing signals. Note that the all logical ones (1's) constant data value which indicates an AIS condition is combined, as described above, with the SONET scrambling pattern to prevent a long sequence of a constant value from occurring in SONET frames. When line terminating equipment at the signal's destination receives and detects the occurrence of the AIS, it responds appropriately to that condition.

During operation of an optical crossconnect in an optical telecommunication system, it is desirable to detect distinct patterns and/or protocols to permit interface fault isolation and/or protection switching. By detecting distinct patterns present in an incoming signal, the optical crossconnect can distinguish between a good signal (a signal with a correct pattern or patterns) and a signal failure (a signal with incorrect or missing patterns). Such pattern detection is applicable even if the average optical power of an input signal to the optical crossconnect remains the same for both a failure condition and a non-failure condition.

Conventional approaches for detecting distinct patterns in a received digital signal usually require recovering a clock signal for the digital modulation present in the received signal, and retiming the data present in that signal. In the instance of optical signals, a small portion of the beam of light carrying the digital data must be optically tapped, i.e. extracting a small fraction of the original signal, to permit pattern and/or protocol detection. Such an optical tap usually extracts 5% to 15% of the power present in the input beam of light thereby providing an optical signal for pattern and protocol detection that is 10 dB to 13 dB less powerful than the signal being monitored. Consequently, a pattern and protocol detector for an optical crossconnect must be capable of operating both with extremely low input power due to low power signal provided by an optical tap, and with extremely low optical to electrical conversion efficiency.

Such a pattern and protocol detector must also be capabl of operating in the presence of erroneous bit values present in the input beam of light. It appears doubtful that conventional clock recovery and data retiming techniques are suitable for use in an optical crossconnect due to a low signal-to-noise ratio resulting from the small amount of power provided by the optical tap. In view of this low signal-to-noise ratio, a conventional clock recovery circuit would likely experience false locking to the clock signal implicitly present in the modulated beam of light, and an increased likelihood of bit errors caused by such false locking.

Disclosure of Invention

The present invention provides simple, high-speed optical signal pattern and protocol detection.

An object of the present invention is to provide an optical crossconnect that is capable of interface fault isolation and/or protection switching.

Another object of the present invention is to permit an optical crossconnect to distinguish between a good signal and a signal failure.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that does not require clock recovery.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that does not require data retiming.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that is capable of operating with a low signal-to-noise ratio.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that is operable with low optical to electrical conversion efficiency.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that operates properly even in the presence of erroneous bit values.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that cannot experience false locking.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that operates with bit rates exceeding 10 Gigabits per second.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that is physically small.

Another object of the present invention is to provide pattern and protocol detection for an optical signal that permits a dense optical crossconnect implementation.

Briefly, the present invention is a pattern and protocol detector for a high-speed optical signal, such as the optical telecommunication signal received by an optical crossconnect. The pattern and protocol detector includes an optical-to-electrical ("OE") converter that receives a modulated beam of light. The modulation is imposed upon the beam of light in accordance with a signal protocol that includes a repetitive pattern. Responsive to impingement of the beam of light, the OE converter produces an electrical-signal.

The pattern and protocol detector also includes a delay means that receives the electrical-signal produced by the OE converter, and that produces a temporally delayed replica of the received electrical-signal. The temporal delay in the electrical-signal introduced by the delay means is selected to effect a matching of the repetitive pattern present in the modulated beam of light between:

a. the electrical-signal produced by the optical-to-electrical converter; and

b. the delayed electrical-signal produced by the delay means.

The pattern and protocol detector also includes a combining circuit that receives both:

a. the electrical-signal produced by the optical-to-electrical converter; and

b. the delayed electrical-signal produced by the delay means.

The combining circuit, preferably an Exclusive-OR gate, combines the received electrical-signal and the delayed electrical-signal to produce a low-frequency signal. The low-frequency signal produced by the combining circuit represents matching and mismatching between individual bits in the received electrical-signal and in the delayed electrical-signal.

Lastly, the pattern and protocol detector includes a digital-logic circuit that receives the low-frequency signal produced by the combining circuit. Responsive to the received low-frequency signal, the digital-logic circuit produces a signal that indicates an occurrence in the beam of light of the repetitive pattern imposed thereon by the modulation.

These and other features, objects and advantages will be understood or apparent to those of ordinary skill in the art from the following detailed description of the preferred embodiment as illustrated in the various drawing figures.

Brief Description of Drawings

FIG. 1 is a block diagram illustrating a redundant optical crossconnect that includes pattern and protocol detectors in accordance with the present invention;

FIG. 2 is a block diagram illustrating a single pattern and protocol detector as may be included in the a redundant optical crossconnect taken along a line 2-2 in FIG. 1;

FIG. 3 is a block diagram illustrating the pattern and protocol detector depicted in FIG. 2 in greater detail including an optical-to-electrical ("OE") converter and a pattern detector circuit thereof;

FIGs. 4A-4E are waveform diagrams illustrating patterns, i.e. low frequency patterns, that occur in the pattern detector circuit depicted in FIG. 3 when the redundant optical crossconnect receives an optical telecommunication signal modulated in accordance with various specific protocols;

FIG. 5 is a block diagram which illustrates an alternative embodiment of the pattern and protocol detector illustrated in FIG. 3 which includes feedback control of the delay introduced by a delay means of the pattern detector circuit, and det cting differing repetitive patterns;

FIG. 6 is a block diagram illustrating a portion of the redundant optical crossconnect depicted in FIG. 1 which illustrates correlating output signals produced by a pair of pattern and protocol detectors to enable operation of the redundant optical crossconnect even if bit errors occur in the optical telecommunication signal;

FIG. 7 is a block diagram illustrating an optical-to-electrical-to-optical ("OEO") regenerator disposed within an optical crossconnect to amplify an optical telecommunication signal before a portion os the signal is extracted for pattern and protocol detection;

FIG. 8 is a block diagram illustrating an optical amplifier disposed within an optical crossconnect to amplify an optical telecommunication signal before a portion os the signal is extracted for pattern and protocol detection; and

FIG. 9 is a block diagram illustrating an amplifier disposed within an optical crossconnect to amplify only that portion of an optical telecommunication which has been extracted for pattern and protocol detection.

Best Mode for Carrying Out the Invention

FIG. 1 depicts a redundant optical crossconnect, referred to by the general reference character 10, adapted for inclusion in a fiber optic telecommunications network. The redundant crossconnect 10 includes two optical switch cores 32a and 32b. Each of the optical switch cores 32a and 32b is preferably of the type disclosed in Patent Cooperation Treaty ("PCT") WO 00/20899 published 13 April 2000, entitled Flexible, Modular, Compact Fiber Optic Switch" that is incorporated herein by reference. As illustrated in FIG. 1, optical telecommunication signals enter the redundant crossconnect 10 at opposite sides thereof via input optical fibers 34a and 34b. Correspondingly, optical telecommunication signals leave the redundant crossconnect 10 at opposite sides thereof via output optical fibers 36a and 36b.

The redundant crossconnect 10 includes a pair of splitter-combiner circuits 38 each of which receives an incoming optical telecommunication signal from one of the input optical fibers 34a or 34b, splits the received optical telecommunication

signal in half, and directs the two halves of the incoming optical telecommunication signal respectively onto one of the optical switch cores 32a and 32b via one of input optical fibers 42aa, 42ba, 42ab and 42bb. Correspondingly, each of the splitter-combiner circuits 38 receives an optical telecommunication signal from one of the optical switch cores 32a and 32b via one of output optical fibers 44aa, 44ba, 44ab and 44bb, combines the optical telecommunication signals received from two output optical fibers 44 into a single signal to produce an outgoing optical telecommunication signal, and directs the outgoing optical telecommunication signal respectively into the corresponding output optical fibers 36a or 36b.

FIG. 1 also illustrates efficacious locations for incorporating four (4) pairs of pattern and protocol detectors 50 into the redundant crossconnect 10. Disposed in these locations, the pattern and protocol detectors 50 can detect distinct patterns and/or protocols that are present in optical telecommunication signals both before and after such signals traverse the optical switch cores 32a and 32b. Monitoring the optical telecommunication signals within the redundant crossconnect 10 in this way with pattern and protocol detectors 50 permits distinguishing between a good signal (a signal with a correct pattern or patterns) and a signal failure (a signal with incorrect or missing patterns). Such pattern detection is applicable even if the average optical power of an input signal to the optical crossconnect remains the same for both a failure condition and a non-failure condition.

While the block diagram of FIG. 1 illustrates only a single pair of input optical fibers 34a and 34b, and a single pair of output optical fibers 36a and 36b, a completely configured redundant crossconnect 10 that includes the present invention may permit simultaneously receiving incoming optical telecommunication signals from hundreds and even thousands of input optical fibers 34, while simultaneously delivering outgoing optical telecommunication signals to hundreds and even thousands of output optical fibers 36. In such a fully configured redundant crossconnect 10, every set of input optical fibers 42aa, 42ba, 42ab and 42bb and output optical fibers 44aa, 44ba, 44ab and 44bb

included therein is equipped as depicted in FIG. 1 with four (4) pairs of pattern and protocol detectors 50. Thus, a fully configured redundant crossconnect 10 includes twice as many pattern and protocol detectors 50 as there are input optical fibers 34 and output optical fibers 36, i.e. hundreds, and even thousands of pattern and protocol detectors 50.

As depicted in a more detailed illustration in FIG. 2, each pattern and protocol detector 50 requires that an optical coupler 52 be inserted into each of the input optical fibers 42 of the redundant crossconnect 10 as indicated in FIG. 2, and also into each of the output optical fibers 44. For pattern detection purposes, the optical coupler 52 optically taps a small portion, e.g. 5% to 15%, from the optical telecommunication signal passing along the input optical fiber 42 or the output optical fiber 44, and redirects the extracted optical signal along an optical fiber 54 to the pattern and protocol detector 50. Because the optical coupler 52 diverts only a small portion of the optical telecommunication signal to the pattern and protocol detector 50, the optical telecommunication signal available there is 10 dB to 13 dB lower than the optical telecommunication signal being monitored. Accordingly, the pattern and protocol detector 50 must operate with extremely low input power due to low value optical tap.

As depicted in FIG. 2, the pattern and protocol detector 50 includes an optical-to-electrical ("OE") converter 56. The OE converter 56 produces at its output a high-frequency, serial electrical-signal which is equivalent to the optical telecommunication signal being monitored. During operation within the redundant crossconnect 10, it is anticipated that the high-frequency, serial electrical-signal produced by the OE converter 56 operates in the 100's of MHz to 10's of GHz range. The pattern and protocol detector 50 also includes a pattern detector 58 that receives the high-frequency, serial electrical-signal produced by the OE converter 56, and produces a signal which indicates when a specific type of repetitive pattern occurs in that signal.

The block diagram of FIG. 3 depicts the pattern and protocol detector 50 in greater detail as adapted to receive the small

portion of the optical telecommunication signal via the optical fiber 54. The OE converter 56 include a high-speed photodetector 66, that is preferably either a PIN diode, or an avalanche photodiode ("APD"). Within the OE converter 56, an amplifier 64 receives the high-frequency, serial electrical-signal produced by the high-speed photodetector 66, amplifies that signal, and transmits the amplified signal both to a delay means 66, and to a combining circuit 68, both of which are included in the pattern detector 58.

The delay means 66 produces a temporally delayed replica of the high-frequency, serial electrical-signal received by the delay means 66. The temporal delay introduced in the high-frequency, serial electrical-signal introduced by the delay means 66 is selected to effect a matching of a repetitive pattern that is present in the modulated beam of light used for the optical telecommunication signal. The combining circuit 68 combines the received high-frequency, serial electrical-signal and the delayed high-frequency, serial electrical-signal to thereby produce a low-frequency serial-pattern signal that represents matching and mismatching between individual bits in the two signals. The the delay imposed by the delay means 66 is selected to produce a low-frequency serial-pattern in the signal produced by the combining circuit 68 that has a detectable steady state behavior. This steady state behavior occurs due to the repetitive pattern(s) present in a particular protocol used to modulate the beam of light that constitutes the optical telecommunication signal.

The combining circuit 68 is preferably a 'single gate' gallium arsenide ("GaAs"), silicon germanium ("SiGe"), or silicon ("Si") based logic circuit, e.g. an Exclusive-OR gate. The combining circuit 68 processes the delayed and non-delayed signals, and then for a properly chosen delay produces a predictable pattern at its the output. SiGe and Si are preferred device technologies for the Exclusive-OR gate combining circuit 68 due to their lower pow r dissipation. The electrical signal produced by the combining circuit 68 is available for processing by a lower speed digital-logic circuit 82, such as a complementary metal-oxide-silicon ("CMOS") field programmable gate array ("FPGA"). If the delay means 66 introduces a delay between the

delayed and non-delayed signals which effects a matching of the SONET framing signal repetitive pattern, then the CMOS FPGA 72 must be capable of detecting only an 8 KHz signal output from the combining circuit 68. Similarly, if the received optical telecommunication signal indicates that an AIS condition has occurred, and if the delay means 66 introduces a delay between the delayed and non-delayed signals which effects a matching of the SONET scrambling pattern, again the CMOS FPGA 72 need only be capable of detecting an 8 KHz signal output from the combining circuit 68.

A digital logic circuit configured into the CMOS FPGA 72 recognizes the low-frequency serial-pattern present in the output signal generated by the combining circuit 68 resulting from the temporal delay introduced by the delay means 66. For a beam of light modulated in accordance with the SONET OC-192 protocol, a passive delay line, such as a printed Circuit board trace, could be used for the delay means 66. To delay the high-frequency, serial electrical-signal for matching of the scrambling pattern requires a reasonable amount of passive delay. The most flexible method for providing the temporal delay is a tunable delay line that is adjustable to different repetitive pattern lengths. A delay line that is adjustable to different repetitive pattern lengths permits adapting the pattern and protocol detector 50 to detect repetitive patterns having differing characteristics. In particular, a Gallium Arsenide, SiGe, or Si application specific integrated circuit ("ASIC") could be used to provide an adjustable delay that is programmable. The temporal delay provided by such an ASIC can be programmed directly via either a serial or parallel interface to the ASIC. The delay chosen and programmed into such an ASIC depends upon the specific repetitive pattern present in the modulation imposed upon the beam of light carrying the optical telecommunication signal received by the redundant crossconnect 10.

The waveform diagrams of FIGs. 4A-4E illustrate patterns that exist on the output of the combining circuit 68 for various different SONET modulation protocols if the combining circuit 68 is implemented using an Exclusive-OR gate. For optical telecommunication signals modulated in accordance with the SONET

protocol, each of the patterns illustrated in FIGs. 4A-4E repeat every 125 microseconds ("μsec"). The illustrations of FIGs. 4A-4E present several optical telecommunication signals that the redundant crossconnect 10 will likely receive.

FIG. 4A depicts the signal produced by the Exclusive-OR gate combining circuit 68 responsive to the occurrence of a framing signal in an optical telecommunication signal that is modulated in accordance with the OC-48 protocol. A vertical line 102 in FIG. 4A indicates an instant at which the $F6_h$ framing signal value first occurs in the optical telecommunication signal. As indicated in FIG. 4A, until the first $F6_h$ framing signal byte propagates to the output of the delay means 66, it is likely that some matching and mismatching will occur between individual bits received by the Exclusive-OR gate combining circuit 68. After the $F6_h$ framing signal value propagates to the output of the delay means 66, the output signal produced by the Exclusive-OR gate combining circuit 68 begins a logical zero (0) value interval because there exists a perfect match between bits in both signals received by the combining circuit 68. The perfect match condition continues for the remainder of the forty-eight (48) $F6_h$ framing signal bytes until the instant, indicated by a vertical line 104 in FIG. 4A, at which the 28_h framing signal value first appears in the output signal produced by the OE converter 56. After the 28_h framing signal value is first received by the Exclusive-OR gate combining circuit 68, there occurs an interval during which both matches and mismatches occur between bits until the first 28_h framing signal value propagates to the output of the delay means 66. After the 28_h framing signal value propagates to the output of the delay means 66, the output signal produced by the Exclusive-OR gate combining circuit 68 resumes a logical zero (0) value interval because there exists a perfect match between bits in both signals received by the combining circuit 68. The perfect match condition continues until the until an instant, indicated by a vertical line 106 in FIG. 4A, at which the last of the forty-eight (48) 28_h framing signal bytes appears in the output signal produced by the OE converter 56. For an optical telecommunication signal modulated in accordance with the OC-48 protocol, this pattern of two long

duration, predictable logical zero (0) states repeat every 125 μsec.

Thus, the presence of the two long duration, predictable logical zero (0) states at the output of the Exclusive-OR gate combining circuit 68 indicates the presence of a framing pattern in an optical telecommunication signal received by the redundant crossconnect 10 that modulated in accordance with the OC-48 protocol. Similar long duration logical zero (0) states occur at the output of the Exclusive-OR gate combining circuit 68 for other SONET protocols. A circuit may be readily configured into the CMOS FPGA 72 that will recognize when these two long duration, predictable logical zero (0) states occur in the output signal received from the Exclusive-OR gate combining circuit 68.

FIG. 4B illustrates the output signal produced by the Exclusive-OR gate combining circuit 68 which results when the redundant crossconnect 10 receives all logical ones (1's) data because an AIS condition has occurred, and the delay means 66 delays the signal produced by the OE converter 56 for an interval equal to the length of the scrambling pattern. In the Illustration of FIG. 4B, the OE converter 56 begins producing the scrambled all logical ones (1's) data at a vertical line 112. As indicated in FIG. 4B, until the first logical one (1) propagates to the output of the delay means 66, it is likely that some matching and mismatching will occur between individual bits received by the Exclusive-OR gate combining circuit 68. After the first logical one (1) propagates to the output of the delay means 66, the output signal produced by the Exclusive-OR gate combining circuit 68 begins a logical zero (0) value interval because there exists a perfect match between bits in both signals received by the combining circuit 68. The perfect match condition continues for the remainder of the all logical ones (1's) until the instant, indicated by a vertical line 114 in FIG. 4B, at which the first framing signal value first appears in the output signal produced by the OE converter 56. For an optical telecommunication signal modulated in accordance with the OC-48 protocol, the predictable logical zero (0) state resulting from an AIS condition repeats every 125 μsec, i.e. at an 8 KHz rate. Again, a circuit may be readily configured into the CMOS FPGA 72

that will recognize when the long duration, predictable logical zero (0) states occurs in the output signal received from the Exclusive-OR gate combining circuit 68 which indicates the occurrence of an AIS condition.

It is significant that, in general, differing temporal delays are required to obtain the long duration, predictable logical zero (0) states illustrated respectively in FIG. 4A for the framing signal, and in FIG. 4B for the AIS condition. Consequently, depending upon the temporal delay selected for the delay means 66, the pattern and protocol detector 50 illustrated in the block diagram of FIG. 3 can produce one or the other, but not both, of the long duration, predictable logical zero (0) states respectively illustrated in those FIGs.

Similar to the OC-48 framing signal illustrated in FIG. 4A, FIG. 4C illustrates the output signal produced by the Exclusive-OR gate combining circuit 68 which results from the framing pattern present in an optical telecommunication signal modulated in accordance with the OC-192 protocol. Similar to the OC-48 framing signal illustrated in FIG. 4B, FIG. 4D illustrates the output signal produced by the Exclusive-OR gate combining circuit 68 which results when an AIS condition occurs in an optical telecommunication signal modulated in accordance with the OC-192 protocol. Also similar to the OC-48 framing signal illustrated in FIG. 4A, FIG. 4E illustrates the output signal produced by the Exclusive-OR gate combining circuit 68 which results from the framing pattern present in an optical telecommunication signal modulated in accordance with the IP over optical protocol.

FIG. 5 illustrates an alternative embodiment of the pattern detector 58 in which the temporal delay introduced by the delay means 66 can be adjusted in response to a control signal. Furthermore, in the alternative embodiment pattern detector 58 depicted in FIG. 5, the CMOS FPGA 72 is configured to generate a control signal which is fed back, via a delay-control signal line 74, to the adjustable delay means 66. Operating in this way, a control signal present on the delay-control signal line 74 controls the temporal delay int rval introduced into the delayed high-frequency, serial electrical-signal by the adjust-

able delay means 66. Such fe dback of a control signal from the CMOS FPGA 72 to the adjustable delay means 66 may be advantageously employed to stabilize operation of the pattern and protocol detector 50 despite changes in temperature, voltage, and device characteristics. Such a feedback loop can also be implemented to select the temporal delay which produces the best operation of the pattern and protocol detector 50. In such an implementation of the pattern and protocol detector 50, analogous to a phase locked loop ("PLL"), the CMOS FPGA 72 can be configured to adjust the temporal delay for the best capture of framing patterns present in an optical telecommunication signal.

Furthermore, the alternative embodiment pattern detector 58 illustrated in FIG. 5 includes a tapped delay means 66. In the illustration of FIG. 5, signal produced by the OE converter 56, delayed to the maximum extent possible by the delay means 66, is received by a first Exclusive-OR gate 68a together with the undelayed signal produced by the OE converter 56. Considering the signals illustrated in FIGs. 4A and 4B, the maximum delay selected for the delay means 66 would be the greater of the delays required for matching of the framing signal or the scrambling pattern. A tap on the delay means 66 transmits a replica of the signal produced by the OE converter 56 delayed a lesser extent which, when supplied to a second Exclusive-OR gate 68b, produces matching of the other signal. In this way, the CMOS FPGA 72 illustrated in FIG. 5 receives from the Exclusive-OR gates 68a and 68b both of the long duration, predictable logical zero (0) states depicted respectively in FIGs. 4A and 4B. By receiving both of these long duration, predictable logical zero (0) states, the CMOS FPGA 72 may be configured to respond appropriately both to the existence of the framing signal in the optical telecommunication signal received by the redundant crossconnect 10, and to receipt of AIS in that signal. While the tapped delay means 66 is preferred, the embodiment of the present invention depicted in FIG. 5 can also be assembled with using two separate delay means which respectively produce the delays described above.

The block diagram of FIG. 6 depicts only a portion of the redundant crossconnect 10 consisting of one-half of one

splitter-combiner circuit 38, only two input optical fibers 42aa and 42ba, and two (2) each of the optical couplers 52, optical fibers 54, OE converters 56, and pattern detectors 58. A double headed arrow 78, extending between the pattern detectors 58 depicted in FIG. 6, indicates correlating output signals between a pair of pattern detectors 58 that are respectively monitoring the same optical telecommunication signal. Correlating output signals between pairs of pattern detectors 58 that respectively monitor the same optical telecommunication signal enables the redundant crossconnect 10 to operate if the input optical telecommunication signal exhibit low optical power, and/or if bit errors occur in the optical telecommunication signal.

Industrial Applicability

The configuration of the redundant crossconnect 10 illustrated in FIG. 1 may be adapted in various ways to improve performance of the pattern and protocol detectors 50 if the redundant crossconnect 10 receives a weak optical telecommunication signal. For example, the block diagram of FIG. 7 depicts inserting an optical-to-electrical-to-optical ("OEO") regenerator 82 preferably into the input optical fiber 42, or into the output optical fiber 44, before the optical coupler 52. Adding the OEO regenerator 82 to the redundant crossconnect 10 strengthens the optical telecommunication signal provided to the pattern and protocol detector 50 by the optical coupler 52. Analogously, the block diagram of FIG. 8 depicts inserting an optical amplifier 84 preferably into the input optical fiber 42, or into the output optical fiber 44, before the optical coupler 52 to strengthen the optical telecommunication signal provided to the pattern and protocol detector 50. The optical amplifier 84 illustrated in FIG. 4 can be implemented as a single amplifier or as a shared amplifier.

Inserting the OEO regenerator 82 or the optical amplifier 84 into the input optical fiber 42 before the optical coupler 52 advantageously strengthens the optical telecommunication signal to overcome signal losses occurring throughout the redundant crossconnect 10. Moreover, inserting the OEO regenerator 82 or the optical amplifier 84 into the input optical fiber 42

strengthens not only the optical tel communication signal supplied to the pattern and protocol detector 50 connected to the input optical fiber 42, but also strengthens the optical telecommunication signal supplied to the pattern and protocol detector 50 connected to the output optical fiber 44.

The block diagram of FIG. 9 depicts inserting an amplifier 86 into the optical fiber 54 between the optical coupler 52 and the OE converter 56. Disposed in this location, the amplifier 86 strengthens only the optical telecommunication signal provided to the pattern and protocol detector 50. In principle, the amplifier 86 may be either an OEO regenerator similar to the OEO regenerator 82 illustrated in FIG. 7, or an optical amplifier similar to the optical amplifier 84 illustrated in FIG. 8. If the amplifier 86 is implemented using an optical amplifier, it may be configured either as a single amplifier or as a shared amplifier. Adding the amplifier 86 in the optical fiber 54 as illustrated in FIG. 9, rather than in the input optical fiber 42 or output optical fiber 44 as illustrated in FIGs. 7 and 8, is advantageous because the amplifier 86 cannot increase the signal-to-noise ratio of the optical telecommunication signal passing through the redundant crossconnect 10.

As is readily apparent from the preceding description of the redundant crossconnect 10, if the received optical telecommunication signal is sufficiently powerful for pattern detection, the OEO regenerator 82, the optical amplifier 84, or the amplifier 86 may be omitted, and the pattern and protocol detector 50 may be simply incorporated into the redundant crossconnect 10 as illustrated in FIGs. 2 and 3.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is purely illustrative and is not to be interpreted as limiting. Consequently, without departing from the spirit and scope of the invention, various alterations, modifications, and/or alternative applications of the invention will, no doubt, be suggested to those skilled in the art after having read the preceding disclosure. Accordingly, it is intended that the following claims be interpreted as encompassing all alterations, modifications, or alternative applications as fall

within the true spirit and scope of th invention.

The Claims

What is claimed is:

1. A pattern and protocol detector for a high-speed optical signal comprising:

an optical-to-electrical converter that:

a. is adapted to receive a beam of light which carries a modulation imposed upon the beam of light in accordance with a signal protocol that includes a repetitive pattern, and

b. responsive to impingement of the beam of light thereon, produces an electrical-signal;

delay means that receives the electrical-signal produced by said optical-to-electrical converter, and that produces a temporally delayed replica of the electrical-signal received by said delay means, the temporal delay in the electrical-signal introduced by said delay means being selected to effect a matching of the repetitive pattern present in the modulated beam of light between:

a. the electrical-signal produced by said optical-to-electrical converter; and

b. the delayed electrical-signal produced by said delay means;

a combining circuit that receives both:

a. the electrical-signal produced by said optical-to-electrical converter; and

b. the delayed electrical-signal produced by said delay means; and

that combines the received electrical-signal and the delayed electrical-signal to thereby produce a low-frequency signal that represents matching and mismatching between individual bits in the electrical-signal and in the delayed electrical-signal as received by said combining circuit; and

a digital-logic circuit that receives the low-frequency signal produced by said combining circuit, and which responsive th reto produces a signal that indicates wh n there occurs in the beam of light the repetitive pattern present in the modulation imposed thereon.

2. The pattern and protocol detector of claim 1 wherein the repetitive pattern present in the modulation imposed on the beam of light includes a framing signal.

3. The pattern and protocol detector of claim 1 wherein the repetitive pattern present in the modulation imposed on the beam of light includes a scrambling pattern.

4. The pattern and protocol detector of claim 1 wherein the repetitive pattern present in the modulation imposed on the beam of light includes both a framing signal and a scrambling pattern.

5. The pattern and protocol detector of claim 1 wherein said optical-to-electrical converter is a PIN diode.

6. The pattern and protocol detector of claim 1 wherein said optical-to-electrical converter is a avalanche photodiode ("APD").

7. The pattern and protocol detector of claim 1 further comprising an amplifier disposed between said optical-to-electrical converter and said delay means, said amplifier:

a. receiving the electrical-signal produced by said optical-to-electrical converter;

b. amplifying the received electrical-signal; and

c. transmitting the amplified electrical-signal to said delay means.

8. The pattern and protocol detector of claim 1 wherein said delay means is a passive delay line.

9. The pattern and protocol detector of claim 8 wherein the passive delay line is a printed circuit board trace.

10. The pattern and protocol detector of claim 1 wherein said delay means is a adjustable delay line.

11. The pattern and protocol detector of claim 10 wherein the temporal delay introduced into the electrical-signal by the adjustable delay line varies in response to a control signal.

12. The pattern and protocol detector of claim 11 wherein said digital-logic circuit also produces a control signal which is supplied to the adjustable delay line for controlling the temporal delay introduced into the electrical-signal by the adjustable delay line.

13. The pattern and protocol detector of claim 1 wherein said delay means includes an application specific integrated circuit ("ASIC").

14. The pattern and protocol detector of claim 13 wherein the ASIC is made from a material selected from a group consisting of gallium arsenide, silicon germanium and silicon.

15. The pattern and protocol detector of claim 13 wherein the temporal delay introduced into the electrical-signal by the ASIC varies in response to a control signal.

16. The pattern and protocol detector of claim 15 wherein said digital-logic circuit also produces a control signal which is supplied to the adjustable delay line for controlling the temporal delay introduced into the electrical-signal by the adjustable delay line.

17. The pattern and protocol detector of claim 1 wherein said combining circuit has a single digital-logic gate.

18. The pattern and protocol detector of claim 17 wh rein the digital-logic gate in an Exclusive-OR gate.

19. The pattern and protocol detector of claim 18 wherein the Exclusive-OR gate is made from a material selected from a group consisting of gallium arsenide, silicon germanium and silicon.

20. The pattern and protocol detector of claim 1 wherein said digital-logic circuit includes a complementary metal-on-silicon ("CMOS") field programmable gate array ("FPGA").

21. The pattern and protocol detector of claim 1 further comprising an optical coupler that:

a. receives an input beam of light which carries the modulation; and

b. extracts a fraction of the received input beam of light for transmission to said optical-to-electrical converter.

22. The pattern and protocol detector of claim 21 further comprising an optical-to-electrical-to-optical regenerator disposed for:

a. receiving the input beam of light before it is received by said optical coupler;

b. amplifying the input beam of light received thereby; and

c. transmitting the amplified input beam of light to said optical coupler.

23. The pattern and protocol detector of claim 21 further comprising an optical amplifier disposed for:

a. receiving the input beam of light before it is received by said optical coupler;

b. amplifying the input beam of light received thereby; and

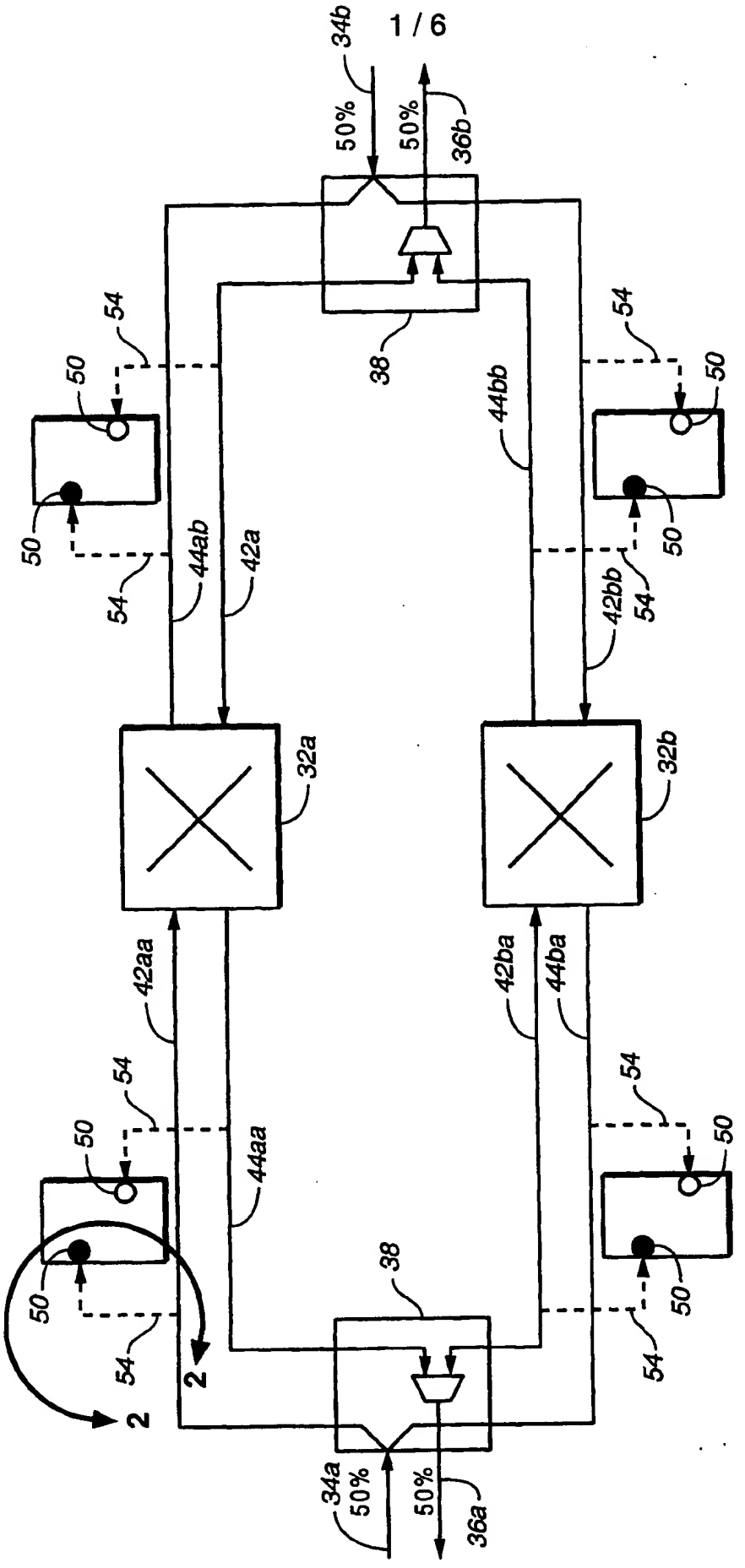
c. transmitting the amplified input beam of light to said optical coupler.

24. The pattern and protocol detector of claim 21 further comprising an optical amplifier disposed between said optical coupler and said optical-to-electrical converter for:

a. receiving the fraction of the received input beam of light extracted by said optical coupler for transmission to said optical-to-electrical converter;

b. amplifying the extracted fraction of the input beam of light received by said optical amplifier; and

c. transmitting the amplified extracted fraction of the input beam of light to said optical-to-electrical converter.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50%
50%
36b
38
54
50
44bb
42a
44ab
42bb
32a
32b
42aa
42ba
44ba
44aa
2
34a
36a
10

FIG._1

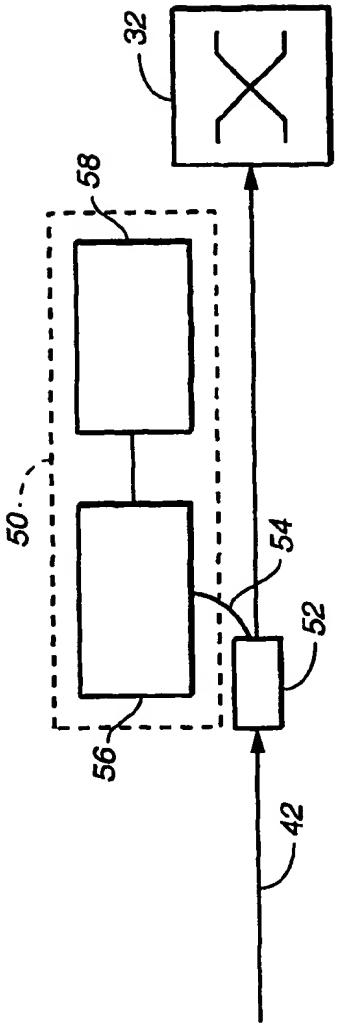


FIG._2

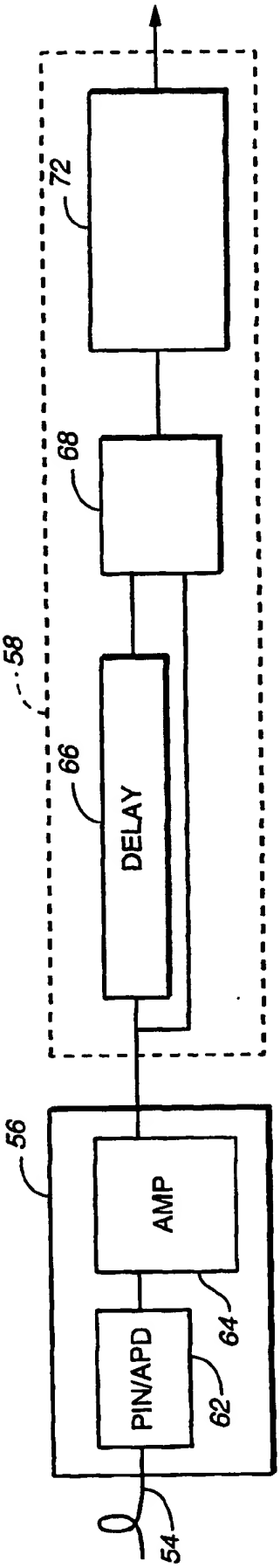


FIG._3

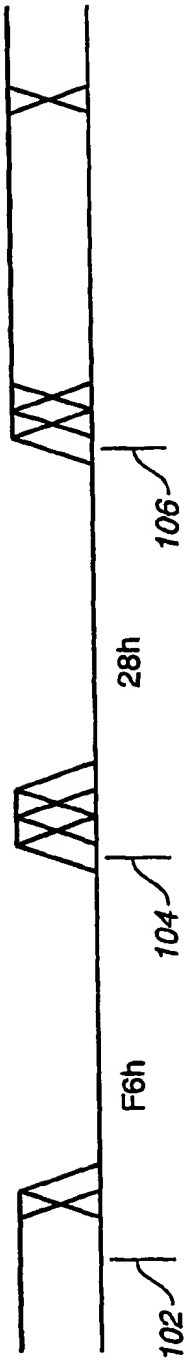


FIG._4A

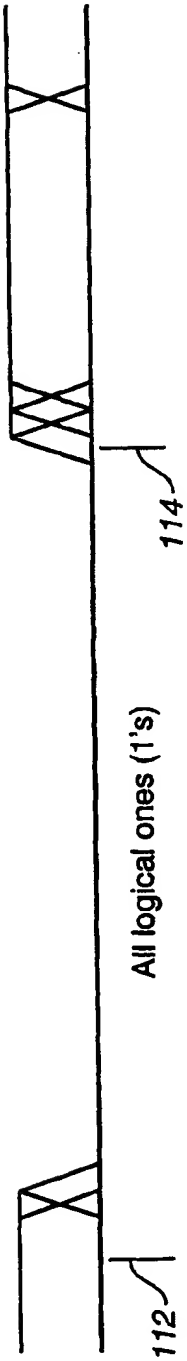


FIG._4B

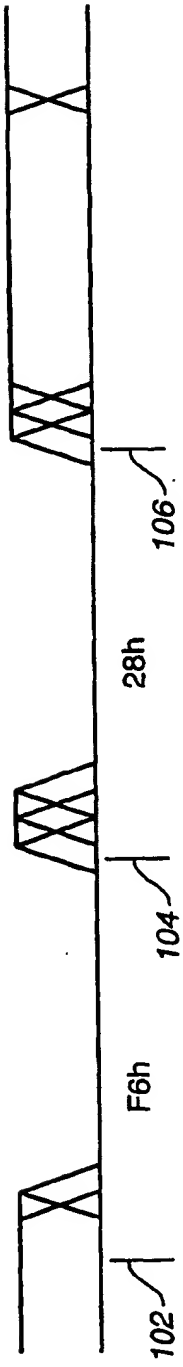


FIG._4C

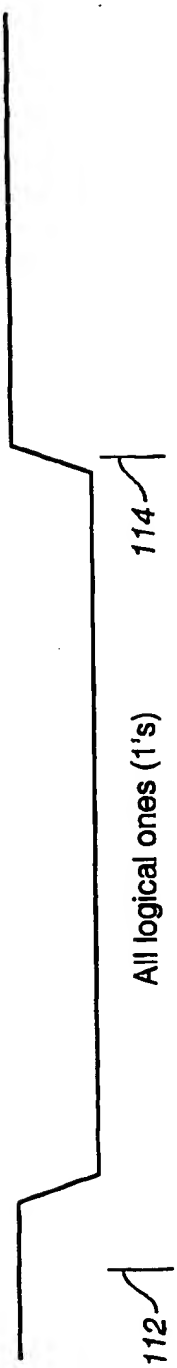


FIG._4D

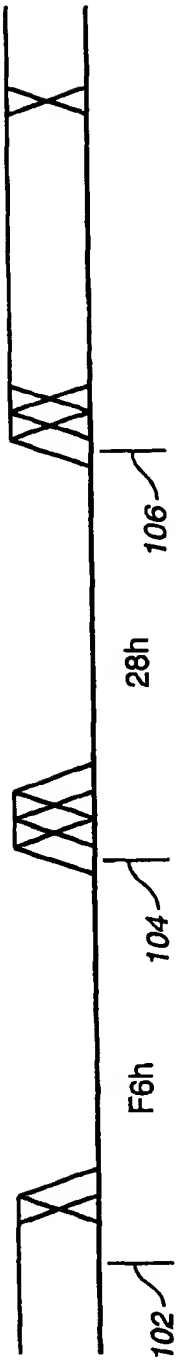


FIG._4E

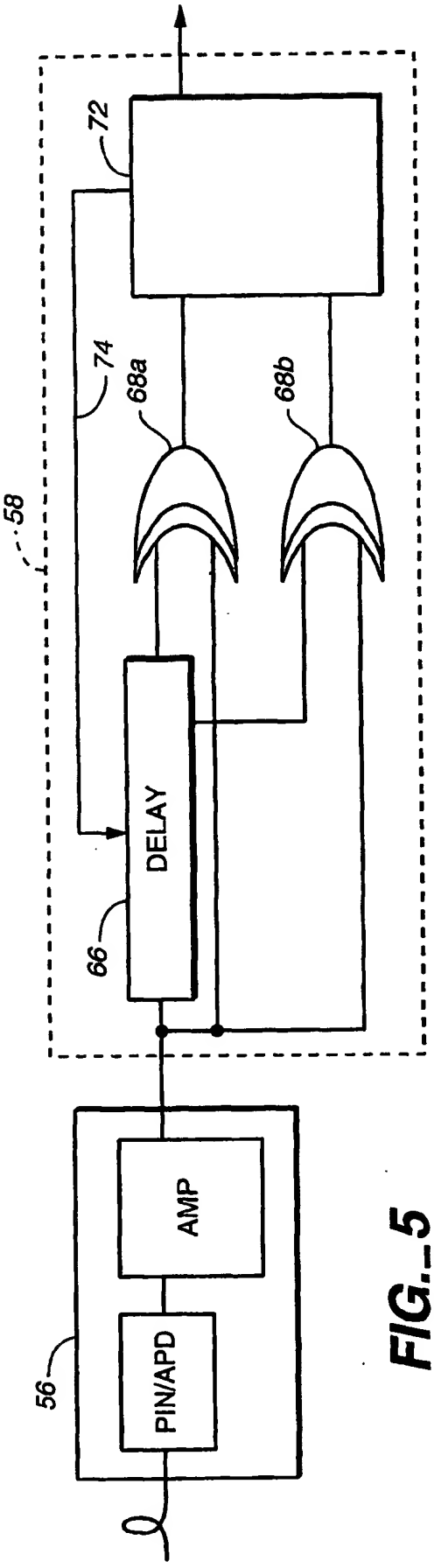
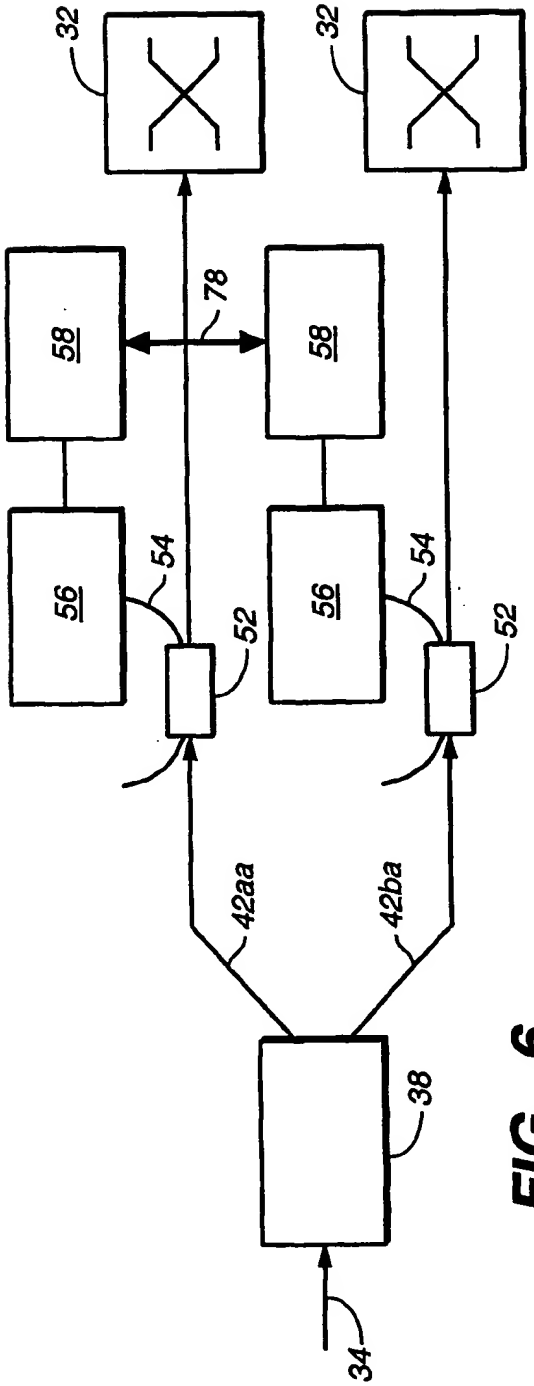

72
74
68a
68b
58
DELAY
66
AMP
PIN/APD
56

FIG._5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42ba
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34

FIG._6

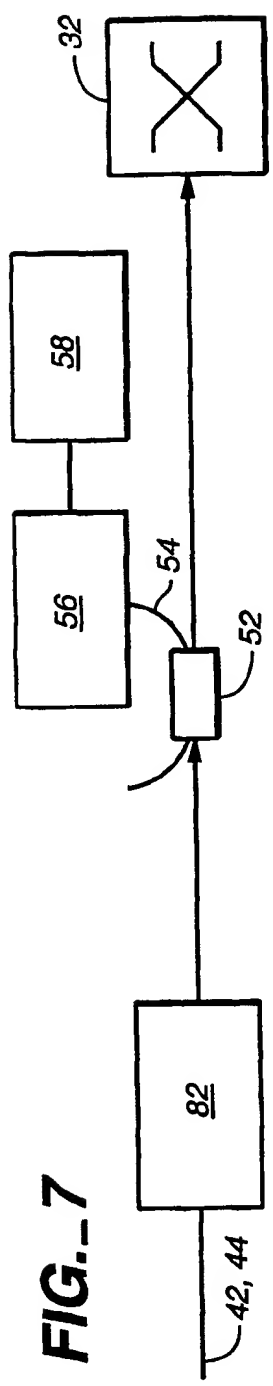

FIG._7

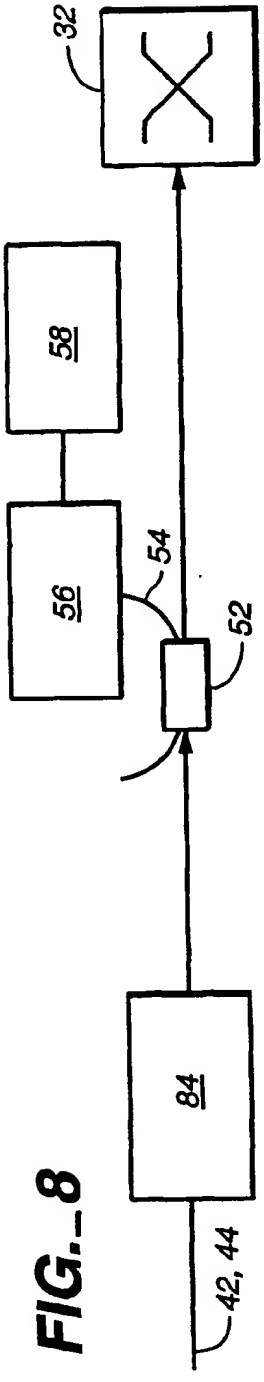

FIG._8

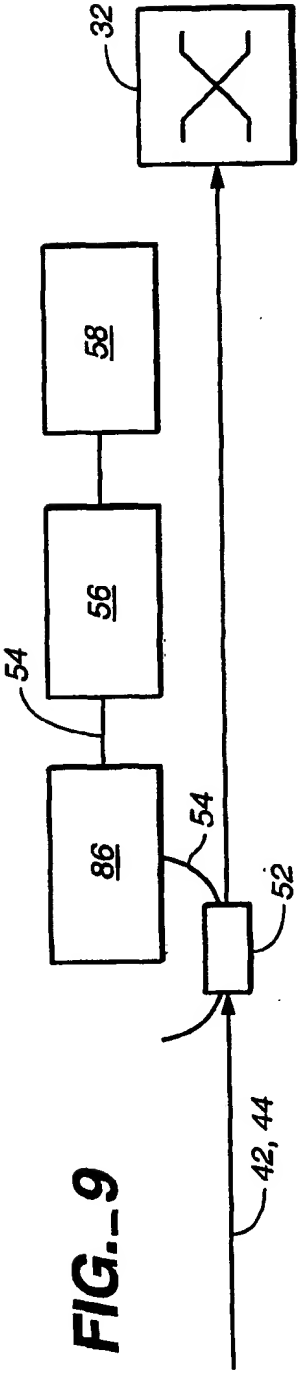

FIG._9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/06019

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H04B 10/06
US CL : 359/189
According t International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 359/189, 110, 177, 140

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y, P	US 6195402 B1 (HIRAMATSU) 27 February 2001 (27.02.2001), entire document.	1-24
Y, P	US 6160821 A (DOLLE et al.) 12 December 2000 (12.12.2000), entire document.	1-24
Y, P	US 6069924 A (SUDO et al.) 30 May 2000 (30.05.2000), entire document.	1-24
Y	US 5942937 A (BELL) 24 August 1999 (24.08.1999), entire document.	1-24
Y	US 5828476 A (BONEBRIGHT et al.) 27 October 1998 (27.10.1998), entire document, particularly columns 13-15.	1-24
Y	US 5719903 A (HIBEN et al.) 17 February 1998 (17.02.1998), entire document.	1-24
Y	US 5694389 A (SEKI et al.) 02 December 1997 (02.12.1997), entire document.	1-24
Y	US 5608735 A (MCCULLOUGH et al.) 04 March 1997 (04.03.1997), entire document.	1-24
Y	US 5349550 A (GAGE) 20 September 1994 (20.09.1994), entire document.	1-24
Y	US 4984238 A (WATANABE et al.) 08 January 1991 (08.01.1991), entire document.	1-24
Y	US 4903225 A (BROST) 20 February 1990 (20.02.1990), entire document.	1-24
Y	US 4817014 A (SCHNEIDER et al.) 28 March 1989 (28.03.1989), entire document.	1-24
Y	US 4563774 A (GLOGE) 07 January 1986 (07.01.1986), entire document.	1-24
Y	US 4369523 A (SEKI et al.) 18 January 1983 (18.01.1983), entire document.	1-24

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Date f the actual completion of the international search
16 May 2001 (16.05.2001)

Date of mailing of the international search report
03 JUL 2001

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